# TOROS ÜNİVERSİTESİ

Faculty Of Engıneerıng
Electrıcal And Electronıcs Engıneerıng (Englısh)

## Course Information

| DIGITAL SYSTEMS AND DESIGN | | | | | |
|---|---|---|---|---|---|
| Code | Semester | Theoretical | Practice | National Credit | ECTS Credit |
| | | Hour / Week | | | |
| EEE205 | Fall | 3 | 2 | 4 | 5 |

| | |
|---|---|
| **Prerequisites and co-requisites** | |
| **Language of instruction** | English |
| **Type** | Required |
| **Level of Course** | Bachelor's |
| **Lecturer** | Asst. Prof. Ziya Gökalp Altun |
| **Mode of Delivery** | Face to Face |
| **Suggested Subject** | |
| **Professional practise ( internship )** | None |
| **Objectives of the Course** | To develop the ability of analyzing combinational and sequential circuits and designing these circuits that satisfy given specifications under realistic conditions. |
| **Contents of the Course** | Digital systems and binary codes, Boolean algebra and logic gates, Karnaugh maps, combinational logic circuits - arithmetic circuits, decoders, encoders, MUX, DEMUX, flip flops, sequential logic circuits - registers, counters. |

## Learning Outcomes of Course

| # | Learning Outcomes |
|---|---|
| 1 | Knowledge of Boolean algebra fundamentals, ability of writing Boolean functions in standard forms and simplifying them using Karnaugh maps. |
| 2 | Ability of analyzing combinational and sequential circuits, and commenting about the functions of these circuits. |
| 3 | Ability of designing combinational or sequential circuits which satisfy given specifications under realistic conditions such as minimum delay time, total count of logic gates etc. |
| 4 | Ability of presenting lab results in a proper technical report format. |

## Course Syllabus

| # | Subjects | Teaching Methods and Technics |
|---|---|---|
| 1 | Number Systems, Binary codes | lecture, discussion, presentation |
| 2 | Boolean Algebra, Logics gates | lecture, discussion, presentation |
| 3 | Boolean functions and canonic forms | lecture, discussion, presentation |
| 4 | Simplification of functions using Karnaugh maps | lecture, discussion, presentation |
| 5 | Analysis and design of combinational circuits | lecture, discussion, presentation |
| 6 | Arithmetic circuits | lecture, discussion, presentation |
| 7 | Magnitute comparators, MUX, DEMUX | lecture, discussion, presentation |
| 8 | Subject repetitions, midterm | |
| 9 | Flip flops | lecture, discussion, presentation |
| 10 | Analysis and design of sequential circuits | lecture, discussion, presentation |

| 11 | Registers | lecture, discussion, presentation |
|---|---|---|
| 12 | Synchronous counters | lecture, discussion, presentation |
| 13 | Ring and Johnson counters, unordered counters | lecture, discussion, presentation |
| 14 | Asynchronous counters, Memory components | lecture, discussion, presentation |
| 15 | | |
| 16 | Final Exam | |

## Course Syllabus

| # | Material / Resources | Information About Resources | Reference / Recommended Resources |
|---|---|---|---|
| 1 | Mano, M. Morris, Digital Design | | |
| 2 | https://madformath.com/calculators/basic-math/base-converters/base-converters | | |

## Method of Assessment

| # | Weight | Work Type | Work Title |
|---|---|---|---|
| 1 | 40% | Mid-Term Exam | Mid-Term Exam |
| 2 | 60% | Final Exam | Final Exam |

## Relationship between Learning Outcomes of Course and Program Outcomes

| # | Learning Outcomes | Program Outcomes | Method of Assessment |
|---|---|---|---|
| 1 | Knowledge of Boolean algebra fundamentals, ability of writing Boolean functions in standard forms and simplifying them using Karnaugh maps. | 2 | 1,2 |
| 2 | Ability of analyzing combinational and sequential circuits, and commenting about the functions of these circuits. | 2,3 | 1,2 |
| 3 | Ability of designing combinational or sequential circuits which satisfy given specifications under realistic conditions such as minimum delay time, total count of logic gates etc. | 3 | 1,2 |
| 4 | Ability of presenting lab results in a proper technical report format. | 4,6,7 | 1,2 |

*PS. The numbers, which are shown in the column Method of Assessment, presents the methods shown in the previous table, titled as Method of Assessment.*

## Work Load Details

| # | Type of Work | Quantity | Time (Hour) | Work Load |
|---|---|---|---|---|
| 1 | Course Duration | 14 | 5 | 70 |
| 2 | Course Duration Except Class (Preliminary Study, Enhancement) | 14 | 4 | 56 |
| 3 | Presentation and Seminar Preparation | 0 | 0 | 0 |
| 4 | Web Research, Library and Archival Work | 0 | 0 | 0 |
| 5 | Document/Information Listing | 0 | 0 | 0 |
| 6 | Workshop | 0 | 0 | 0 |
| 7 | Preparation for Midterm Exam | 1 | 9 | 9 |
| 8 | Midterm Exam | 1 | 1 | 1 |
| 9 | Quiz | 0 | 0 | 0 |
| 10 | Homework | 0 | 0 | 0 |
| 11 | Midterm Project | 0 | 0 | 0 |
| 12 | Midterm Exercise | 0 | 0 | 0 |
| 13 | Final Project | 0 | 0 | 0 |

| 14 | Final Exercise | 0 | 0 | 0 |
|----|----------------|---|---|---|
| 15 | Preparation for Final Exam | 1 | 13 | 13 |
| 16 | Final Exam | 1 | 1 | 1 |
| | | | | **150** |